

What is claimed is:

Sub a1
5 1. A method for manufacturing a semiconductor device comprising:
sequentially forming an interconnection layer, a capping layer, and an etching stopper
on a semiconductor substrate;

forming an interlayer insulating layer having a first contact hole exposing a surface of
the etching stopper formed of a material having a high etching selectivity with respect to the
interlayer insulating layer;

10 forming a second contact hole to substantially expose a top surface of the capping
layer by removing a portion of the etching stopper exposed by the first contact hole; and
forming a conductive layer within the second contact hole.

15 2. The method for manufacturing a semiconductor device of claim 1 further
comprising forming a third contact hole by slightly etching a portion of the capping layer
exposed by the second contact hole before forming a conductive layer, and wherein the
conductive layer is formed within the second contact hole and the third contact hole.

20 3. The method for manufacturing a semiconductor device of claim 2, wherein the
conductive layer is formed only in the second and third contact holes.

25 4. The method for manufacturing a semiconductor device of claim 2, wherein the
conductive layer is an upper interconnection layer filling the second and third contact holes
and covering the top surface of the interlayer insulating layer.

30 5. The method for manufacturing a semiconductor device of claim 2 wherein the
second and third contact holes are formed by performing a dry etching method using an
etchant having a low etching selectivity between the etching stopper and the capping layer.

6. The method for manufacturing a semiconductor device of claim 1, wherein the
etching stopper is formed of an inorganic anti-reflecting layer (ARL) or an organic anti-
reflecting coating (ARC).

7. The method for manufacturing a semiconductor device of claim 1, wherein the
interconnection layer is a metal layer containing aluminum.

B2

8. The method for manufacturing a semiconductor device of claim 1, wherein the capping layer is formed of TiN, Ti/TiN or TaN.

5 9. The method for manufacturing a semiconductor device of claim 1, wherein the interlayer insulating layer is formed of one selected from the group consisting of a silicon oxide layer, a silicon nitride layer, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), tetraethylorthosilicate (TEOS), plasma enhanced TEOS (PE-TEOS), and undoped silicate glass (USG).

10 10. The method for manufacturing a semiconductor device of claim 1, wherein the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers for forming the interconnection layer, the capping layer, and the etching stopper, and patterning the material layers by the same etching process.

15 11. The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is formed only in the second contact hole.

20 12. The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is an upper interconnection layer filling the second contact hole and covering the top surface of the interlayer insulating layer.

25 13. The method for manufacturing a semiconductor device of claim 1, wherein the first contact hole is formed by using a dry etching method.

30 14. A semiconductor device comprising:
a semiconductor substrate;
an interconnection layer formed on the semiconductor substrate;
a capping layer formed on the interconnection layer;
an etching stopper formed on the capping layer;
an interlayer insulating layer having a contact hole overlying the interconnection layer, the contact hole formed through the etching stopper to substantially expose a portion of the capping layer; and
a conductive material layer disposed within the contact hole.

B

15. The semiconductor device of claim 14, wherein the etching stopper is adjacent to sidewalls of the contact hole.

5 16. The semiconductor device of claim 14, the etching stopper is formed of an inorganic anti-reflecting layer (ARL) or an organic anti-reflecting coating (ARC).

17. The semiconductor device of claim 14, wherein the interconnection layer is a metal layer containing aluminum.

10 18. The semiconductor device of claim 14, wherein the capping layer is formed of a material selected from the group consisting of TiN, Ti/TiN, and TaN.

15 19. The semiconductor device of claim 14, wherein the conductive layer is formed only in the contact hole.

20 20. The semiconductor device of claim 14, wherein the conductive layer is an upper interconnection layer filling the contact hole and covering the top surface of the interlayer insulating layer.

add
a3